AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A CMOS operational transconductance amplifier, comprising:

a differential input transistor pair providing an input stage for receiving a pair of input voltages;

a current source, coupled to the differential input transistor pair, for providing current to the differential input transistor pair;

an output transistor for conducting an output current proportional to a difference between the pair of input voltages applied to the differential input transistor pair; [[and]]

a cascode current mirror section, coupled to the differential input transistor pair and the output transistor, the cascode current mirror section providing a mirrored current as the output current for the output transistor, the cascode current mirror section comprising a first current mirror transistor coupled to a drain of a first transistor of the differential input transistor pair and a second current mirror transistor coupled to a drain of a second transistor of the differential input transistor pair, the second current mirror transistor being coupled to the output transistor; and

a common-mode feedback section, coupled to the differential input transistor pair, wherein the common-mode feedback section absorbs a current change in the current source to maintain a constant current in the output transistor, ~~; and wherein~~ the common-mode feedback section ~~comprises~~ comprising a second current source and a common-mode feedback differential pair, a transistor of the common-mode feedback differential pair mirroring current through the first current mirror transistor.

Claims 2-3. (Cancelled)

4. (Currently Amended) The CMOS operational transconductance amplifier of claim [[3]] 1 wherein the second current mirror transistor and the output transistor are scaled to provide a desired current ratio.

Claim 5. (Cancelled)

6. (Currently Amended) The CMOS operational transconductance amplifier of claim [[5]] 1 wherein a transistor of the common-mode feedback differential pair and the first current mirror transistor absorb the current change in the current source to maintain a constant current in the second current mirror transistor.

7. (Currently Amended) The CMOS operational transconductance amplifier of claim [[3]] 1 wherein the cascode current mirror section further comprises an amplifier section for boosting the transconductance of the cascode current mirror section.

8. (Original) The CMOS operational transconductance amplifier of claim 7 wherein the amplifier section comprises a first amplifier coupled to the first current mirror transistor and a second amplifier coupled to the second current mirror transistor.

9. (Currently Amended) The CMOS operational transconductance amplifier of claim [[2]] 1 wherein the cascode current mirror section further comprises an amplifier section for boosting the transconductance of the cascode current mirror section.

10. (Currently Amended) A method for providing high common-mode rejection ratio in a single-ended CMOS operational transconductance amplifier, comprising:

providing an differential input stage; ~~, and~~

providing a current source to the differential input stage;

providing a cascode current mirror section coupled to the differential input stage, wherein providing the cascode current mirror section further comprises providing a first current mirror transistor coupled to a drain of a first transistor of the differential input stage and providing a second current mirror transistor coupled to a drain of a second transistor of the differential input pair, the second current mirror transistor being coupled to the output transistor;

coupling an output transistor to the cascode mirror section to mirror current at the cascode current mirror section;

compensating for a current change caused by a common-mode level change at the input stage to maintain a constant current at an output; and

wherein compensating for a current change further comprises providing a second current source and a common-mode feedback differential pair, a transistor of the common-mode feedback differential pair mirroring current through the first current mirror transistor.

Claims 11-12. (Cancelled)

13. (Currently Amended) The method of claim 10 ~~12~~ wherein the providing the second current mirror transistor and the output transistor further comprises forming the output transistor with a width twice the width of the second current mirror transistor to provide a desired current ratio.

Claim 14. (Cancelled)

15. (Currently Amended) The method of claim 10 ~~14~~ wherein the compensating for a current change further comprises absorbing the current change in the current source using the transistor of the common-mode feedback differential pair and the first current mirror transistor.

16. (Currently Amended) The method of claim 10 ~~11~~ further comprising boosting the transconductance of the cascode current mirror section using an amplifier section.

17. (Original) The method of claim 16 wherein the boosting the transconductance of the cascode current mirror section using an amplifier section further comprises providing a first amplifier coupled to the first current mirror transistor and providing a second amplifier coupled to the second current mirror transistor.

18. (Currently Amended) An analog-to-digital converter (ADC), comprising:

a sample-and-hold circuit for sampling an input analog signal and providing a held sample at an output of the sample-and-hold circuit;

a gain stage, coupled to the output of the sample-and-hold circuit, for amplifying the held sample and providing an amplified signal at an output of the gain stage;

a comparator circuit, coupled to the output of the gain stage, the comparator circuit comparing the amplified signal to a reference signal to provide a digital output based upon the comparison;

wherein at least one of the sample-and-hold circuits, gain stage and comparator circuit includes a CMOS operational transconductance amplifier, the CMOS operational transconductance amplifier comprises:

a differential input transistor pair providing an input stage for receiving a pair of input voltages;

a current source, coupled to the differential input transistor pair, for providing current to the differential input transistor pair;

an output transistor for conducting an output current proportional to a difference between the pair of input voltages applied to the differential input transistor pair; and

a common-mode feedback section, coupled to the differential input transistor pair, wherein the common-mode feedback section absorbs a current change in the current source to maintain a constant current in the output transistor.

19. (Original) The ADC of claim 18 further comprising a cascode current mirror section, coupled to the differential input transistor pair and the output transistor, the cascode current mirror section providing a mirrored current as the output current for the output transistor..

20. (Currently Amended) The ADC of claim 19 wherein the cascode current mirror section comprises a first current mirror transistor coupled to a drain of a first transistor of the differential input transistor pair and a second current mirror transistor coupled to a drain of a second transistor of the differential input transistor pair, the second current mirror transistor being coupled to the output transistor.

21. (Original) The ADC of claim 20 wherein the second current mirror transistor and the output transistor are scaled to provide a current ratio of 1:2.

22. (Original) The ADC of claim 20 wherein the common-mode feedback section comprises a second current source and a common-mode feedback differential pair, a transistor of the common-mode feedback differential pair mirroring current through the first current mirror transistor.

23. (Original) The ADC of claim 22 wherein the transistor of the common-mode feedback differential pair and the first current mirror transistor absorb the current change in the current source to maintain a constant current in the second current mirror transistor.

24. (Original) The ADC of claim 20 wherein the cascode current mirror section further comprises an amplifier section for boosting the transconductance of the cascode current mirror section.

25. (Original) The ADC of claim 24 wherein the amplifier section comprises a first amplifier coupled to the first current mirror transistor and a second amplifier coupled to the second current mirror transistor.

26. (Original) The ADC of claim 19 wherein the cascode current mirror section further comprises an amplifier section for boosting the transconductance of the cascode current mirror section.

Claim 27. (Cancelled)

28. (Currently Amended) A CMOS operational transconductance amplifier, comprising:

a differential input ~~transistor~~ pair providing an input stage;

a current source, coupled to the differential input pair, for providing current to the differential input pair;

an output transistor providing an output current;

a first current mirror transistor coupled to a drain of a first transistor of the differential input pair;

a second current mirror transistor coupled to a drain of a second transistor of the differential input pair, the second current mirror transistor being coupled to the output transistor for providing a mirrored current as the output current for the output transistor;

a second current source; and

a common-mode feedback differential pair, coupled to the second current source and to the first and second current mirror transistors, a transistor of the common-mode feedback differential pair mirroring current through the first current mirror transistor to compensate for a current change in the current source to maintain a constant mirrored current.

29. (Original) The CMOS operational transconductance amplifier of claim 28 wherein the second current mirror transistor and the output transistor are scaled to provide a desired current ratio.

30. (Original) The CMOS operational transconductance amplifier of claim 28 wherein the transistor of the common-mode feedback differential pair and the first current mirror transistor absorb the current change in the current source to maintain a constant current in the second current mirror transistor.